## IN THE CLAIMS

Claims 1-15 are currently pending in the application. Claim 1 is an independent claim and claims 2-15 depend there from. Claims 3-10 and 15 are currently amended to overcome minor informalities noticed by the Examiner. The Applicant respectfully asserts that the minor amendments to claims 3-10 and 15 do not alter the scope of the claims as originally presented, but rather correct minor grammatical errors objected to by the Examiner.

Please amend the claims as follows.

1. (Original) A system for reducing noise in a chip, the system comprising:

a substrate layer integrated within the chip;

a transistor layer integrated within the chip, which is shielded from said substrate layer by a shielding layer;

at least one transistor of a first transistor type that couples said transistor layer to said shielding layer; and

a quiet voltage source that is coupled to said at least one transistor of said first transistor type.

2. (Original) The system according to claim 1, further comprising at least one transistor of a second transistor type coupled to said shielding layer.

3. (Currently Amended) The system according to claim 2, wherein said at least one transistor of ~~a~~ said second transistor type is ~~a~~ an n-type transistor.

4. (Currently Amended) The system according to claim 2, wherein said at least one transistor of ~~a~~ said second transistor type is disposed within said transistor layer.

5. (Currently Amended) The system according to claim 2, wherein said at least one transistor of ~~a~~ said second transistor type is resistively coupled to said shielding layer.

6. (Currently Amended) The system according to claim 2, further comprising a first noisy voltage source coupled to said at least one transistor of ~~a~~ said second transistor type.

7. (Currently Amended) The system according to claim 6, wherein said first noisy voltage source is coupled to a source of said at least one transistor of ~~a~~ said second transistor type.

8. (Currently Amended) The system according to claim 1, wherein said at least one transistor of ~~a~~ said first transistor type is a p-type.

9. (Currently Amended) The system according to claim 1, wherein said at least one transistor of ~~a~~ said first transistor type is disposed within said transistor layer.

10. (Currently Amended) The system according to claim 1, wherein said at least one transistor of ~~a~~ said first transistor type is capacitively coupled to said shielding layer.

11. (Original) The system according to claim 1, wherein said shielding layer is capacitively coupled to said substrate layer.

12. (Original) The system according to claim 1, wherein said shielding layer is disposed between said substrate layer and said transistor layer.

13. (Original) The system according to claim 1, wherein said shielding layer is a deep N-well.

14. (Original) The system according to claim 1, further comprising a second noisy voltage source coupled to said at least one transistor of a first transistor type.

15. (Currently Amended) The system according to claim ~~6~~ 14, wherein said second noisy voltage source is coupled to a source of said at least one transistor of a first transistor type.